



ATTORNEY DOCKET NO. 28951.5186

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Confirmation No.: 4222

Takaki YOSHIDA et al.

Group Art Unit: 2133

Serial No.: 09/697,305

Examiner: Joseph D. Torres

Filed: October 27, 2000

For: FAULT DETECTING METHOD AND
LAYOUT METHOD FOR SEMICONDUCTOR
INTEGRATED CIRCUIT

CONFIRMATION OF TELEPHONE ELECTION

Director, U.S. Patent & Trademark Office
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Sir:

The Examiner in charge of the above-identified application telephoned applicants' representatives on September 12, 2005, to communicate a restriction requirement between Group I (claims 5, 6, 10 and 11) and Group II (claims 7, 8, 9, 13, 19 and 20).

In response to that restriction requirement, applicants' undersigned representatives made a provisional election during a telephone conference with the Examiner on September 15, 2005 to prosecute the invention of Group II (claims 7, 8, 9, 13, 19 and 20) in this application. Applicants' undersigned representative hereby confirms that this provisional election was specifically made with traverse, since no adequate basis therefor has yet been set forth in the record.

Respectfully submitted,

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